PATENT ABSTRACTS OF JAPAN

(11)Publication number : 04-351024
(43)Date of publication of application : 04.12.1992

(51)Int.Cl. H04B 17/00
G01R 29/08

(21)Application number : 03-123999
(22)Date of filing : 28.05.1991

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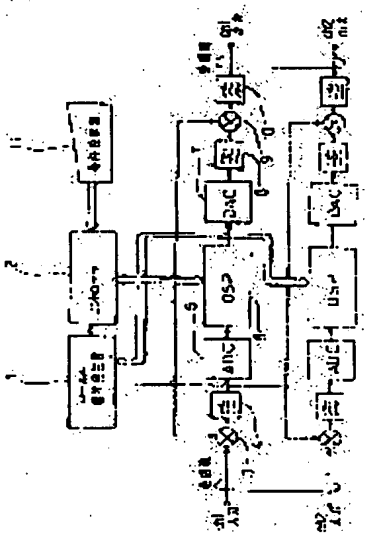
(54) MULTI-PATH FADING SIMULATOR

(57)Abstract:
PURPOSE: To realize diversified multi-path fading simulation accurately and easily by providing an A/D converter, a digital signal processing section and a D/A converter to the simulator so as to analyze the multi-path fading by digital signal processing.
CONSTITUTION: One channel is constituted of a mixer 3, low pass filter 4, A/D converter 5, digital signal processor 6, D/A converter 7, low pass filter 8, mixer 9 and band pass filter 10, and plural channels are provided as required, and the characteristic is controlled entirely by using the controller 2 to which the simulation condition is given from a condition setting device 11. Through the constitution above, a local signal from a local signal generator 1 is mixed with a processing signal by using the mixers 3,9 to implement frequency conversion, and the mixer 3 converts the signal into an intermediate frequency signal within a band of the converter 5, and the mixer 9 decodes conversely the signal into the original RF signal. Thus, the degree of freedom is expanded and the simulation is easily and accurately implemented.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

(19)日本国特許庁（ＪＰ）　(12)**公開特許公報（Ａ）**　(11)特許出願公開番号

特開平6－104855

(43)公開日　平成６年(1994)４月15日

(51)Int.Cl.[5]	識別記号	庁内整理番号	ＦＩ	技術表示箇所
Ｈ０４Ｂ　17/00		Ｃ　7170－5Ｋ		

審査請求　未請求　請求項の数１(全　６　頁)

(21)出願番号　特願平4－246762

(22)出願日　平成４年(1992)９月16日

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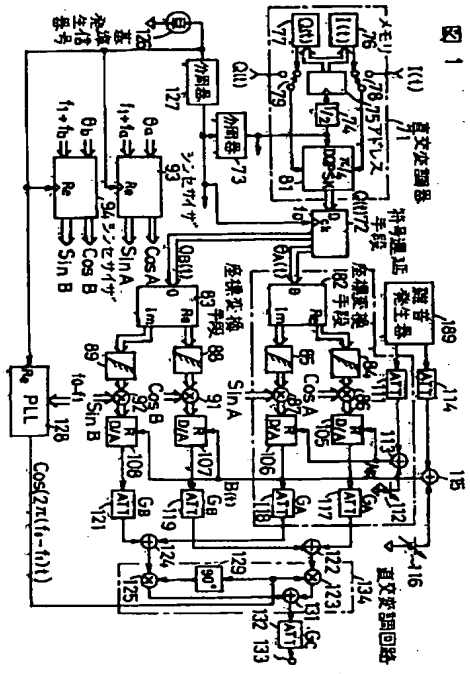
(54)【発明の名称】　フェージングシュミレータ

(57)【要約】　（修正有）
【目的】温度変動の影響を受けにくく、高周波数の平衡変調器や位相シフタを必要とせず、調整しやすくする。
【構成】フェージングシュミレーションの場合は、符号遅延手段７２の同一シフト段から２つの伝送符号θ$_B$（ｔ）とθ$_B$（ｔ）を得、又は２つの符号が相関を保つ状態でわずかに遅延量をずらせる。第一電波通路と第二電波通路における各ドプラーシフトはｆａ，ｆｂとしてそれぞれシンセサイザ９３，９４に与えられ、２つの電波通路の位相差は設定位相θａ，θｂによって決定され、レイリー雑音はＡ（ｔ），Ｂ（ｔ）で与えられ、減衰量は減衰器１１７，１１９によって変化させる。隣接チャネル間の干渉信号を得るには、符号遅延手段より出力される２つの信号θ$_A$（ｔ）とθ$_B$（ｔ）とが相関が無い程度に相互に遅延量の差を大きくし、その状態でシンセサイザの設定周波数の一部ｆａとｆｂとを十分に離してチャネル間の周波数差を得る。

図１



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【特許請求の範囲】

【請求項１】　送信符号のステップ遅延を実現する符号遅延手段と、

位相及び周波数可変な第一、第二デジタルシンセサイザーと、

上記符号遅延手段からの２つの符号出力のそれぞれについて第一実部と第一虚部の第二実部と、第二虚部をそれぞれ得る第一、第二座標変換手段と、

上記第一実部及び第一虚部にそれぞれ上記第一シンセサイザーの余弦波出力、正弦波出力をそれぞれ掛け算する第一、第二掛け算手段と、

上記第二実部、第二虚部に上記第二シンセサイザーの余弦波出力、正弦波出力をそれぞれ掛け算する第三、第四掛け算手段と、

上記第一、第二掛け算手段の出力にそれぞれ雑音を掛け算すると共に、アナログ信号に変換する第一、第二ＤＡ変換手段と、

上記第三、第四掛け算手段に上記雑音と異なる雑音をそれぞれ掛け算すると共にアナログ信号に変換する第三、第四ＤＡ変換手段と、

上記第一、第三ＤＡ変換手段の各出力を加算する第一加算手段と、

上記第二、第四ＤＡ変換手段の各出力を加算する第二加算手段と、

上記第一加算手段及び第二加算手段の出力を直交変調する変調手段と、

を具備するフェージングシュミレータ。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】この発明は、デジタル移動通信システムなどの受信性能を評価するために用いられ、レイリー散乱を受けたり、ドプラーシフトを受けたり、フェージングを受けた状態の信号と同様な信号をリアルタイムで発生するフェージングシュミレータに関する。

【０００２】

【従来の技術】図３に従来のフェージングシュミレータを示す。同相信号Ｉ（ｔ）と直交信号Ｑ（ｔ）とが直交変調器１１に加えられ、その変調出力は極座標から直交座標へ変換する座標変換器１２においてその実部と虚部とに変換（分割）される。これら変換された実部及び虚部はデジタルの低域通過フィルタ１３，１４をそれぞれ通じて乗算型のＤＡ変換器１５，１６にそれぞれ供給される。ＤＡ変換器１５，１６の基準電圧源に可変直流電源１７の出力電圧が印加されて直流電圧V_Aが掛け算される。

【０００３】これらＤＡ変換器１５，１６の出力はそれぞれ掛け算器１８，１９に供給され、正弦波発振器２１からの周波数f_Aの搬送波出力がそのまま掛け算器１８に供給されると共に９０度移相回路２２を通じて掛け算器１９に供給され、これら掛け算器１８，１９の出力は

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加算器２３で加算され、その加算出力、つまり直交変調出力は掛け算器２４において、ランダム雑音発生器２５からの雑音が減衰器２６で適当なレベルとされた雑音Ａ（ｔ）と掛け算される。この雑音が掛けられた信号は減衰器２７でG_Aだけ減衰され、その減衰された出力は可変遅延手段２８によりt_Aだけ遅延されて掛け算器２９に供給されると共に移相器３１を通じて掛け算器３２に供給される。正弦発振器３３より周波数f_1の信号が掛け算器２９に供給されると共に９０度移相器３４を通じて掛け算器３２に供給される。掛け算器２９，３２の出力は加算器３５で加算される。

【０００４】一方、加算器２３の出力は分岐されて切り替えスイッチ３６の固定接点Ｆ側を通じて掛け算器３７にも供給される。掛け算器３７には雑音発生器２５からの雑音が減衰器３８を通じて雑音Ｂ（ｔ）として与えられている。この掛け算器３７の出力は減衰器３９によりG_Bだけ減衰され、さらにその減衰出力は可変遅延手段４１によりt_Bだけ遅延されて掛け算器４２へ供給される。周波数f_2の正弦波を発生する発振器４３の出力が掛け算器４２に供給されると共に９０度移相器４４を通じて掛け算器４５に供給され、遅延手段４１の出力はフェイズシフタ４６を通じて掛け算器４５も供給される。掛け算器４２，４５の各出力は加算器４７で加算される。加算器３５，４７の各出力が加算器４８により加算され、その加算出力は減衰器４９でG_Cだけ減衰を受けて出力端子５１に出力される。

【０００５】また、同相信号Ｉ′（ｔ）及び直交信号Ｑ′（ｔ）が直交変調器５２において搬送波を直交変調し、その変調出力が座標変換器５３において実部と虚部とに変換され取り出され、これら実部及び虚部はデジタルの低域通過フィルタ５４，５５をそれぞれ通じて乗算型のＤＡ変換器５６，５７へ供給される。ＤＡ変換器５６，５７には可変電源５８より電圧V_Bが基準電源端子に印加されてV_Bが掛け算される。ＤＡ変換器５６，５７の各出力はそれぞれ掛け算器５９，６１へ供給され、発振器６２からの周波数f_Bの搬送波が掛け算器５９に供給されると共に９０度移相器６３を通じて掛け算器６１へ供給される。掛け算器５９，６１の出力は加算器６４で加算され、その加算出力は切り替えスイッチ３６の固定接点Ｉ側を通じて掛け算器３７に供給される。

【０００６】移動局と固定局または移動局間の通信においては直接波と反射波とが同時に受信され、しかもその反射波はレベルと位相が変動し、あるいは複数の反射波が主として受信される。このため受信信号はレベル及び位相が変動したものとなる。また移動局と固定局間の相対的移動により受信周波数がいわゆるドプラーシフトにより変動する。これら変動状態を、シュミレーション（フェージングシュミレーション）するには切り替えスイッチ３６を固定接点Ｆ側とに接続しておく。この時出力端子５１に得られる出力信号は次式で表される。

【0007】$G_c \cdot \{G_A \cdot A(t) \cdot \cos\{2\pi(f_A + f_1) \cdot (t - t_A) + \theta_A(t)\} \cdot V_A + G_B \cdot B(t) \cdot \cos\{2\pi(f_A + f_2) \cdot (t - t_B) + \theta_A(t)\} \cdot V_A\}$

ここでA（t）は電波の第一通路のレイリー散乱であり、B（t）は電波の第二通路のレイリー散乱と等価である。また減衰量G_A，G_Bはそれぞれ第一，第二通路の減衰量である。f_Aが搬送波周波数であり、f_1，f_2がそれぞれ第一，第二通路におけるドプラーシフト周波数である。またθ_A（t）は送信情報である。さらにt_A，t_Bはそれぞれ第一，第二通路の時間遅れである。よってこれらの各部の減衰量あるいは遅延手段28，41の遅延量t_A，t_Bまた周波数f_1，f_2などを変化させることによっていろいろな状態つまり、実際にフェージングを受けた状態をシュミレートすることができる。

【0008】一方隣接チャネル間の干渉をシュミレートするには切り替えスイッチ36を固定接点I側に接続する。この状態における出力端子51の出力は次式で表される。

$G_c \cdot \{G_A \cdot A(t) \cdot \cos\{2\pi(f_A + f_1) \cdot (t - t_A) + \theta_A(t)\} \cdot V_A + G_B \cdot B(t) \cdot \cos\{2\pi(f_B + f_2) \cdot (t - t_B) + \theta_B(t)\} \cdot V_B\}$

ここでθ_B（t）はチャネルB側の送信情報である。f_BはチャネルB側の搬送波周波数である。この場合隣接チャネル間においては搬送波周波数が$f_A + f_1$と$f_B + f_2$間の干渉となり且つこれらの時間ないし位相は遅延手段28，41によって調整され、その周波数差はf_1，f_2，f_A，f_Bによって変更され、レベルはG_A，G_Bで変更される。

【0009】

【発明が解決しようとする課題】従来においては、2つの通路差を変更するため可変遅延手段28，41が用いられているが、この遅延時間t_A，t_Bを得るには通常、線路いわゆるケーブルの遅延時間を利用しているため温度変動にしたがって遅延時間が変化し、また周波数によって遅延歪みが生じ、さらに高い分解能で広い範囲によって遅延時間を変化することが難しい。

【0010】また多数の高周波数の平衡変調器つまり掛け算器18，19，24，29，32，37，42，45，59，61を使用しており、さらに多くの高周波の位相シフタを使用しているため、周波数に対する調整が難しい。しかも2つの系統が用いられ構成が複雑となっていた。

【0011】

【課題を解決するための手段】この発明によれば、符号遅延手段から送信符号がステップ的に遅延され、その2つの遅延出力の各符号について第一実部と第一虚部、第二実部と第二虚部が第一、第二座標交換手段により変換

され、これら第一実部、第一虚部は第一デジタルシンセサイザーからの余弦波出力及び正弦波出力とそれぞれ第一、第二掛け算手段によって掛け算され、またこれら第一、第二掛け算手段の出力はそれぞれ第一、第二乗算型DA変換手段によって雑音が掛けられると共にアナログ信号に変換される。一方第二実部、第二虚部は第二デジタルシンセサイザーよりの余弦波出力と正弦波出力がそれぞれ第三、第四掛け算手段によって掛け算され、これら第三、第四掛け算出力は第三、第四乗算型DA変換手段によって、上記とことなる雑音が掛け算されると共にアナログ信号に変換される。第一、第三DA変換手段の出力が第一加算手段で加算され、第二、第三、第四DA変換手段の出力は第二加算手段で加算され、これら第一、第二加算手段の出力が直交変調手段で直交変調される。

【0012】

【実施例】図1にこの発明の実施例を示す。直交変調器71からの送信情報θ（t）は、符号遅延手段72に供給されてその符号単位即ちステップ的遅延が行われる。符号遅延手段72は例えばシフトレジスターやFIFOメモリなどが用いられる。また直交変調器71としてはデーター発生用クロック発生器73よりのデーター発生用クロックが分周器74で1／2に分周され、その分周出力がアドレスカウンタ75で計数され、そのアドレスカウンタ75の計数値をアドレスとして同相用メモリ76、直交用メモリ77がそれぞれ読みだされて同相信号I（t）と直交信号Q（t）とが出力される。これら両出力がそれぞれ切り替えスイッチ78，79を通じて変調器81へ供給され搬送波長、例えばπ／4DQPSK変調する。スイッチ78，79は外部からの同相信号及び直交信号を入力する場合に切り替えられる。

【0013】符号遅延手段72よりそれぞれ符号単位でことなる遅延が与えられた、あるいは同一の遅延が与えられた信号が出力される。符号遅延手段72が例えばシフトレジスタの場合は異なるタップ（シフト段）からの出力あるいは同一タップ（シフト段）からの出力がそれぞれ符号送信情報θ_A（t）と、θ_B（t）として取り出され、座標変換手段82，83へ供給される。座標変換手段82，83において各入力符号はそれぞれ極座標、直交座標の変換が行われて実部と虚部がそれぞれ出力される。座標変換手段82からの実部及び虚部はそれぞれ必要に応じてFIR形デジタル低域通過フィルタ84，85を通じて乗算器86，87へ供給される。また座標変換手段83よりの実部及び虚部はそれぞれ必要に応じてFIR形デジタル低域通過フィルタ88，89を通じて乗算器91，92に供給される。

【0014】一方デジタルシンセサイザー93，94が設けられる。デジタルシンセサイザー93，94はそれぞれ位相及び周波数を変化することができるもので、例えば図2Aに示すように構成される。即ちトグル型のフ

リップフロップ９５からの周波数f_sが１／２とされた一方の出力によりラッチ回路９６に加算器９７の出力をラッチする。加算器９７はラッチ回路９６の出力と周波数データk_fとを加算する。またラッチ回路９６の出力は位相データ$k\theta$と加算回路９８で加算され、その出力は、移相回路９９において０度の位相または９０度の位相シフトが与えられて、正弦波メモリ１０１へ読み出しアドレスとして供給される。正弦波メモリ１０１には正弦波形の各サンプル点のレベルが記憶されており、その読み出されたデジタルの正弦波信号は、ラッチ回路２６に対するラッチ指令によってラッチ回路１０２にラッチされ、またこのラッチ指令に対して１８０度位相がずれた信号によってラッチ回路１０３にラッチされる。ラッチ回路１０２の出力がデジタル正弦波出力となり、ラッチ回路１０３の出力がラッチ回路２６に対するラッチと同時にラッチ回路１０４にラッチされ、ラッチ回路１０４からデジタルの余弦波出力が得られる。周波数データk_fが周波数f_s／２のクロックごとに累積加算されるため、周波数データk_fが大きいほど周波数が高くなり、周波数データk_fが小さいほど周波数は低くなる。移相回路９９はそのまま出力するか、９０度位相をずらして出力するものであるから図２Ｂに示すように、その入力データの最上位のビットと次のビットをそのまま通過するか、それらを排他的論理和を取ったものを最上位ビットとし、最上位から２番目のビットを反転したものを最上位から２番目のビットとして出力するかの切り替えを行えばよい。このようにして周波数が$f_s \times k_f \div 2^{L+1}$、位相$\theta$が$2\pi \times k\theta \div 2^{L}$の正弦波出力と余弦波出力とが得られる。$f_s$はフリップフロップ９５を駆動するクロックの周波数である。

【００１５】図１の説明に戻って、シンセサイザー９３に対して周波数$f_1 + f_a$が設定され、位相θ_aが設定され、これにより余弦波出力$\cos\{2\pi(f_1 + f_a)t + \theta_a\}$が出力されて乗算器８６に供給され、また正弦波出力$\sin\{2\pi(f_1 + f_a)\cdot t + \theta_a\}$が出力されて乗算器８７に供給される。一方シンセサイザー９４に対しては周波数$f_1 + f_b$が設定され、位相θ_bが出力され、その余弦波出力$\cos\{2\pi(f_1 + f_b)\cdot t + \theta_b\}$が乗算器９１に供給され、正弦波出力$\sin\{2\pi(f_1 + f_b)\cdot t + \theta_b\}$が乗算器９２に供給される。乗算器８６，８７の各出力はそれぞれ乗算型ＤＡ変換器１０５，１０６に供給され、また乗算器９１，９２の各出力はそれぞれ乗算型ＤＡ変換器１０７，１０８に供給される。一方ランダム雑音発生器１０９よりランダム雑音が発生され、その雑音は必要に応じて減衰器１１１にて減衰された後、可変直流電源１１２よりの直流電圧と加算回路１１３で加算され、その加算回路１１３の出力がレイリー雑音Ａ（ｔ）として乗算型ＤＡ変換器１０５，１０６の各基準電源端子に供給されてその入力デジタル信号と掛け算されると共に、そのデジタル信号がアナログ信号に変換される。

同様に雑音発生器１０９からの雑音が減衰器１１４を通じて加算器１１５に供給されて可変直流電源１１６の出力直流電圧とが加算され、加算器１１５からの出力がレイリー雑音Ｂ（ｔ）として乗算器ＤＡ変換器１０７，１０８の基準電源端子に供給されて、その入力デジタル信号に対して掛け算されると共にそのデジタル信号をアナログ信号に変換される。

【００１６】ＤＡ変換器１０５，１０６の各出力はそれぞれ減衰器１１７，１１８においてそれぞれＧａずつ減衰され、またＤＡ変換器１０７，１０８よりの各出力は減衰器１１９，１２１においてそれぞれG_sだけ減衰される。減衰器１１７，１１９の出力は加算器１２２において加算されて乗算器１２３に供給され、また減衰器１１８，１２１の各出力は加算器１２４で加算されて乗算器１２５に供給される。

【００１７】基準信号発生器１２６よりの信号は周波数f_sであってシンセサイザー９３，９４にそれぞれクロックとして供給されると共に、その出力は分周器１２７により整数分の１に分周されてデータ発生用クロック発生器２７に供給されると共に、符号遅延手段７２に対するシフトクロックとして供給され、その他のデジタル処理のためのクロックとして各部に供給される。さらに基準信号発生器１２６の出力は位相ロックループ（ＰＬＬ）１２８に基準信号として供給され、そのＰＬＬ１２８には搬送波周波数$f_0 - f_1$が設定入力され、基準信号と同期した周波数$f_0 - f_1$の信号$\cos\{2\pi(f_0 - f_1)\cdot t\}$が出力され、これが搬送波信号として乗算器１２３に供給されると共に９０度移相器１２９を通じて乗算器１２５に供給される。乗算器１２３，１２５の出力は加算器１３１で加算され、その加算出力は減衰器１３２にて減衰されて出力端子１３３に出力される。乗算器１２３，１２５、移相器１２９、加算器１３１は直交変調回路１３４を構成している。またＰＬＬ１２８の出力搬送波周波数を$f_0 - f_1$とするのは出力端子１３３の出力信号の搬送波周波数f_0を増加したり減少する必要があり、つまりシンセサイザー９３，９４において負の周波数を発生することができないから、f_1だけ高い周波数として、それに対して正、負の周波数f_a，f_bを自由に選ぶことができ、これによりその直交変調回路１３における出力搬送波の周波数を中心f_0に対し、正にも負にもf_a，f_bだけ変化することができる。

【００１８】この構成においては、符号遅延手段７２にシフトレジスタを使用し、そのシフト周波数をf_sとし、出力が取り出されるシフト段をn_a，n_bとすると、座標変換手段８２，８３に供給される符号情報はそれぞれ$\theta_a(t) = \theta(t - n_a/f_d)$、$\theta_b(t) = \theta(t - n_b/f_d)$となる。よって端子１３３により出力される信号は次のようになる。

【0019】Gc・〔Ga・A（t）・cos｛2π（f。＋fa）・t＋θa＋θ（t－na／fd）｝＋Gb・B（t）・cos｛2π（f。＋fb）・t＋θb＋θ（t－nb／fd）｝〕

フェージングシュミレーションの場合は符号選出手段72における同一シフト段から、2つの伝送符号θ$_A$（t）とθ$_B$（t）を得、または伝送符号θ$_A$（t）、θ$_B$（t）が相関を保つ状態においてわずか遅延量をずらす。2つの電波の通路にたいするレイリー散乱がA（t）とB（t）として与えられ、その第一の電波通路と第二電波通路における各ドプラーシフトはfa，fbとしてそれぞれ小さな値が与えられる。その2つの電波通路の位相差はデジタルシンセサイザー93，94における設定位相θa，θbにより決定され、レイリー雑音はA（t），B（t）で与えられ、減衰量は減衰器117，119によって変化させられる。第一電波通路の遅れ時間は｛（na／fd）－θa／2π（f。＋fa）｝で与えられ、第二電波通路の時間遅れは｛（nb／fd）－θb／2π（f。＋fb）｝で与えられる。このようにすることによって各部を制御し従来技術と同様にフェージング効果が与えられた信号を得ることができる。

【0020】また隣接チャネル間の干渉信号を得る場合においては、符号遅延手段27においてこれより出力される2つの信号θ$_A$（t）とθ$_B$（t）とが相関が無い程度に相互に遅延量の差を大とし、その状態においてチャネル間の周波数差を得るためにシンセサイザー93，94の設定周波数の一部faとfbとを互いに十分離す。この場合も従来と同じように隣接チャネル間の干渉信号をシュミレーションすることができる。

【0021】上述において、座標変換手段82、フィルター84，85、乗算器86，87、DA変換器105，106、減衰器111、加算器113、減衰器117，118、電源112の組を複数箇設けることによってマルチパスフェージングのシュミレーションやその他多数チャネル間の干渉シュミレーションを行うことができる。また上述においては、π／4DQPSK変調信号についてのフェージングシュミレーションを行ったが変調器71を変更することによって他の通信方式に対するフェージングや隣接チャネル間干渉のシュミレーションを行うこともできる。

【0022】

【発明の効果】以上述べた様に、この発明によれば2つの通路の差や隣接チャネル干渉の信号通路の差を符号遅延手段72における遅延の差と、周波数シンセサイザー93，94における設定位相の差等を利用してデジタル的に作るため、従来のように遅延線路を使用していないため周囲温度の変動によって影響されることがなく、連続的かつ広範囲にわたって温度や周波数変化に対して安定で歪みのない伝送遅延シュミレーションを行うことが可能である。また比較的低い周波数でレイリー散乱やドプラーシフトの処理をデジタル的に実現しているため、高い周波数での平衡変調器や位相シフタはわずか終段における直交変調回路134のみでよく、よって周波数に対する調整が容易である。

【図面の簡単な説明】

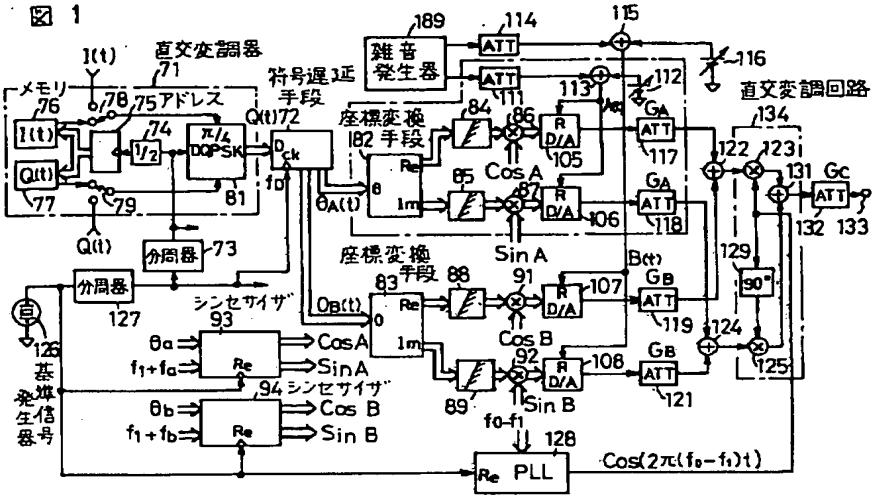
【図1】この発明の実施例を示すブロック図。

【図2】Aはデジタルシンセサイザーの例を示すブロック図、Bはその移相回路99を示すブロック図である。

【図3】従来のフェージングシュミレータを示すブロック図。

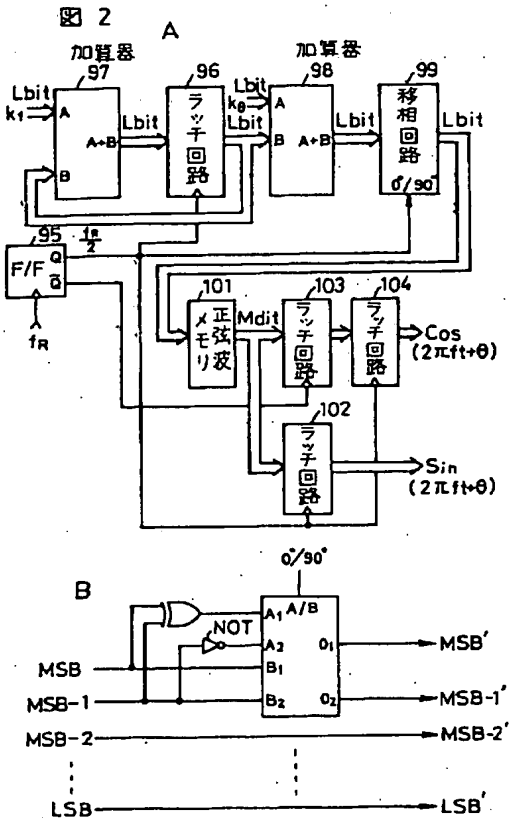
【図1】

図 1



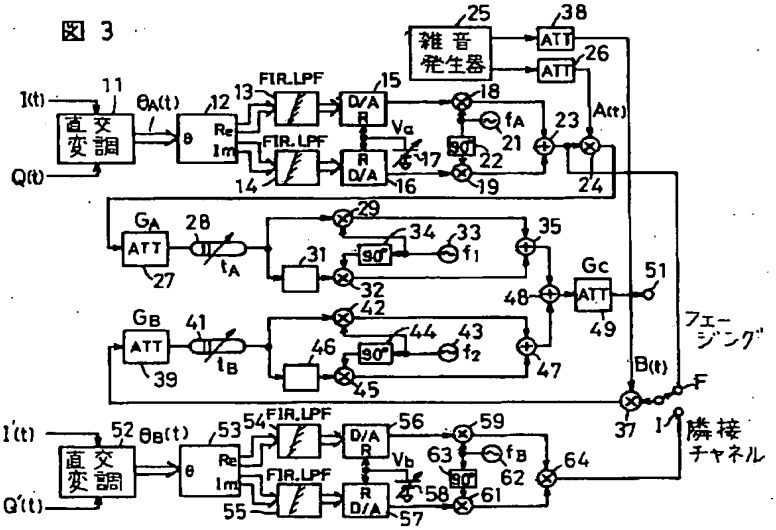
【図2】

図 2


A
加算器
97
96
ラッチ回路
加算器
98
99
移相回路
Lbit
k1
kθ
A
B
A+B
0°/90°
95
F/F
Q
Q̄
fR
fo/2
101
正弦波メモリ
Mdit
103
104
102
Cos (2πft+θ)
Sin (2πft+θ)
B
NOT
A/B
A1
A2
B1
B2
O1
O2
MSB
MSB-1
MSB-2
LSB
MSB'
MSB-1'
MSB-2'
LSB'

【図3】

図 3


I(t)
Q(t)
直交変調
θA(t)
Re
Im
FIR.LPF
D/A
Vα
fA
fB
f1
f2
GA
GB
GC
ATT
90°
雑音発生器
25
38
26
A(t)
B(t)
フェージング
隣接チャネル
I'(t)
Q'(t)
θB(t)
Vb
F
1

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CLAIMS

[Claim(s)]
[Claim 1] A sign delay means to realize step delay of a transmitting sign, and the strange first with good phase and frequency and the second digital synthesizer, About each of two sign outputs from the above-mentioned sign delay means, the first real part and the second real part of the first imaginary part, A first and second coordinate transformation means to obtain the second imaginary part, respectively, and a first and second multiplication means to multiply the first real part of the above, and the first imaginary part by the cosine wave output of the first synthesizer of the above, and the sinusoidal output, respectively, While multiplying the output of a third and fourth multiplication means to multiply the second real part of the above, and the second imaginary part by the cosine wave output of the second synthesizer of the above, and the sinusoidal output, respectively, and the above-mentioned first and second multiplication means by the noise, respectively The first changed into an analog signal, the second DA translation means, and a third and fourth DA translation means to change into an analog signal while multiplying the above-mentioned third and fourth multiplication means by the above-mentioned noise and different noise, respectively, The phasing simulator possessing a first addition means to add each output of the third DA translation means for a start [above-mentioned], a second addition means to add each output of the above-mentioned second and fourth DA translation means, and the modulation means that carries out quadrature modulation of the output of the above-mentioned first addition means and the second addition means.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention is used in order to evaluate receiving engine performance, such as digital migration communication system, and receive Rayleigh scattering, a Doppler shift is received, or it relates phasing to the phasing simulator generated on real time in the signal of a carrier beam condition, and the same signal.
[0002]
[Description of the Prior Art] The conventional phasing simulator is shown in drawing 3 . In-phase signal I (t) and rectangular signal Q (t) is added to the quadrature modulation machine 11, and the modulation output is changed into the real part and imaginary part in the coordinate transformation machine 12 changed into rectangular coordinates from a polar coordinate (division). The real part and imaginary part which were these-changed are supplied to DA converters 15 and 16 of a multiplication mold respectively through the digital low pass filters 13 and 14, respectively. The output voltage of adjustable DC power supply 17 is impressed to the source of reference voltage of DA converters 15 and 16, and it is direct current voltage VA. It multiplies.
[0003] The output of these DA converters 15 and 16 is supplied to multipliers 18 and 19, respectively. Frequency fA from a sine wave oscillator 21 While a subcarrier output is supplied to a multiplier 18 as it is, a multiplier 19 is supplied through a phase-shifting circuit 22 90 degrees. The output of these multipliers 18 and 19 is added with an adder 23, and it multiplies by the addition output, i.e., a quadrature modulation output, in a multiplier 24 with noise A (t) by which the noise from the random noise generator 25 was made suitable level with the attenuator 26. the signal with which this noise was imposed -- an attenuator 27 -- GA only -- it decreases -- having -- that decreased output -- the adjustable delay means 28 -- tA only -- while being delayed and supplying a multiplier 29, a multiplier 32 is supplied through a phase shifter 31. It is a frequency f1 from the sine oscillator 33. While a signal is supplied to a multiplier 29, a multiplier 32 is supplied through a phase shifter 34 90 degrees. The output of multipliers 29 and 32 is added with an adder 35.
[0004] On the other hand, the output of an adder 23 branches and is supplied also to a multiplier 37 through the stationary-contact F side of a changeover switch 36. The noise from a noise generator 25 is given to the multiplier 37 as noise B (t) through the attenuator 38. the output of this multiplier 37 -- an attenuator 39 -- GB only -- it decreases -- having -- further -- that attenuation output -- the adjustable delay means 41 -- tB only -- it is delayed and a multiplier 42 is supplied. Frequency f2 While the output of the oscillator 43 which generates a sine wave is supplied to a multiplier 42, a multiplier 45 is supplied through a phase shifter 44 90 degrees, and as for the output of the delay means 41, a multiplier 45 is also supplied through the phase shifter 46. Each output of multipliers 42 and 45 is added with an adder 47. each output of adders 35 and 47 adds with an adder 48 -- having -- the addition output -- an attenuator 49 -- GC only -- in response to attenuation, it is outputted to an output terminal 51.
[0005] Moreover, in-phase signal I' (t) and rectangular signal Q' (t) carry out quadrature modulation of the subcarrier in the quadrature modulation machine 52, in the coordinate

transformation machine 53, the modulation output is changed into real part and imaginary part, and is taken out, and these real part and imaginary part are supplied to DA converters 56 and 57 of a multiplication mold respectively through the digital low pass filters 54 and 55. In DA converters 56 and 57, it is an electrical potential difference VB from the adjustable power source 58. It is impressed by the criteria power supply terminal, and is VB. It multiplies. Multipliers 59 and 61 are supplied and each output of DA converters 56 and 57 is the frequency fB from an oscillator 62, respectively. While a subcarrier is supplied to a multiplier 59, a multiplier 61 is supplied through a phase shifter 63 90 degrees. The output of multipliers 59 and 61 is added with an adder 64, and the addition output is supplied to a multiplier 37 through the stationary-contact I side of a changeover switch 36.

[0006] In the communication link between a mobile station, a fixed station, or a mobile station, a direct wave and a reflected wave are received simultaneously, and moreover, as for the reflected wave, level and a phase are changed, or two or more reflected waves are mainly received. For this reason, an input signal becomes that to which level and a phase were changed. Moreover, received frequency is changed by the so-called Doppler shift by the relative movement between a mobile station and a fixed station. For carrying out the simulation (phasing simulation) of these fluctuation condition, the changeover switch 36 is connected to the stationary-contact F side. The output signal acquired by the output terminal 51 at this time is expressed with a degree type.

[0007] GC - [-- GA - A -- (-- t --) - cos -- {-- two -- pi (fA+f1) - (t-tA) -- + -- theta -- A -- (-- t --) --} - VA -- + -- GB - B -- (-- t --) - cos -- {-- two -- pi (fA+f2) - (t-tB) -- + -- theta -- A -- (-- t --) --} - VA --]

A (t) is Rayleigh scattering of the first path of an electric wave, and its B (t) is equivalent to Rayleigh scattering of the second path of an electric wave here. Moreover, the magnitude of attenuation GA and GB It is the magnitude of attenuation of the second path for a start, respectively. fA It is carrier frequency and is f1 and f2. It is a Doppler shift frequency in the second path for a start, respectively. Moreover, thetaA (t) is transmit information. Furthermore, they are tA and tB. It is the time lag of the second path for a start, respectively. therefore, the magnitude of attenuation of these each part or the amount tA of delay of the delay means 28 and 41, and tB again -- a frequency f1 and f2 etc. -- making it change -- various conditions -- that is, a carrier beam condition can be actually simulated for phasing.

[0008] For, simulating interference between adjacent channels on the other hand, a changeover switch 36 is connected to a stationary-contact I side. The output of the output terminal 51 in this condition is expressed with a degree type.

GC - [-- GA - A -- (-- t --) - cos -- {-- two -- pi (fA+f1) - (t-tA) -- + -- theta -- A -- (-- t --) --} - VA -- + -- GB - B -- (-- t --) - cos -- {-- two -- pi (fB+f2) - (t-tB) -- + -- theta -- B -- (-- t --) --} - VB --]

It is thetaB here. (t) is the transmit information by the side of Channel B. fB It is the carrier frequency by the side of Channel B. In this case, it sets between adjacent channels and carrier frequency is fA+f1. fB+f2 It becomes interference of a between, and these time amount thru/or phases is adjusted by the delay means 28 and 41, and that frequency difference is f1, f2, fA, and fB. It is changed and level is GA and GB. It is changed.

[0009]

[Problem(s) to be Solved by the Invention] Although the adjustable delay means 28 and 41 are used in the former in order to change two path differences, they are this time delay tA and tB. It is difficult for a time delay to change according to temperature fluctuation, since the time delay of a line ******** cable is usually used for obtaining, and for delay distortion to arise with a frequency and to change a time delay with large range with still higher resolution.

[0010] Moreover, since it is used, many the balanced modulators 18, 19, 24, 29, 32, 37, 42, 45, 59, and 61, i.e., the multipliers, of high frequency, and the phase shifter of much more RFs is used, the adjustment to a frequency is difficult. And two systems were used and the configuration was complicated.

[0011]

[Means for Solving the Problem] According to this invention, a transmitting sign is delayed from

a sign delay means in step. The first real part, the first imaginary part and the second real part, and the second imaginary part about each sign of the two delay outputs The first, It is changed by the second coordinate operator stage. These first real part and the first imaginary part, respectively with the cosine wave output from the first digital synthesizer, and a sinusoidal output The first, It multiplies with the second multiplication means, and for a start [these], the output of the second multiplication means is changed into an analog signal, respectively while a noise is imposed by the second multiplication mold DA translation means for a start. on the other hand, the cosine wave output and the sinusoidal output from the second digital synthesizer multiply by the second real part and the second imaginary part with the third and fourth multiplication means, respectively -- having -- these third and fourth multiplication output -- the third and fourth multiplication mold DA translation means -- the above -- things -- it is changed into an analog signal while a noise multiplies. For a start, the output of the third DA translation means is added with the first addition means, the output of the second, third, and fourth DA translation means is added with the second addition means, and quadrature modulation of the output of the second addition means is carried out with a quadrature modulation means for a start [these].

[0012]

[Example] The example of this invention is shown in drawing 1 . Transmit information [from the quadrature modulation machine 71] theta (t) is supplied to the sign delay means 72, and the sign unit, i.e., step-delay, is performed. As for the sign delay means 72, a shift register, a FIFO memory, etc. are used. Moreover, as a quadrature modulation machine 71, dividing of the clock for data generating from the clock generation machine 73 for data generating is carried out to one half with a counting-down circuit 74, counting of the dividing output is carried out with an address counter 75, the memory 76 for inphases and the memory 77 for a rectangular cross are read considering the enumerated data of the address counter 75 as the address, respectively, and in-phase signal I (t) and rectangular signal Q (t) is outputted. both [these] outputs supply a modulator 81 through changeover switches 78 and 79, respectively -- having -- subcarrier length -- for example, a pai-fourth-Differential-QPSK modulation is carried out. Switches 78 and 79 are changed when inputting the in-phase signal and the rectangular signal from the outside.

[0013] the sign delay means 72 -- respectively -- a sign unit -- things -- delay was given or the signal with which the same delay was given is outputted. The output from a tap (shift stage) which is different when the sign delay means 72 is a shift register, or the output from the same tap (shift stage) is sign transmit information thetaA, respectively. (t) and thetaB It is taken out as (t) and the coordinate transformation means 82 and 83 are supplied. In the coordinate transformation means 82 and 83, conversion of a polar coordinate and rectangular coordinates is performed and, as for each input sign, real part and imaginary part are outputted, respectively. The real part and imaginary part from the coordinate transformation means 82 are supplied to multipliers 86 and 87 through the FIR form digital low pass filters 84 and 85 if needed, respectively. Moreover, the real part and imaginary part from the coordinate transformation means 83 are supplied to multipliers 91 and 92 through the FIR form digital low pass filters 88 and 89 if needed, respectively.

[0014] On the other hand, the digital synthesizers 93 and 94 are formed. The digital synthesizers 93 and 94 are constituted, as it can change and a phase and a frequency are shown in drawing 2 A, respectively. Namely, frequency fR from the flip-flop 95 of a toggle mold While was set to one half and the output of an adder 97 is latched to a latch circuit 96 with an output. An adder 97 is the output and the frequency data kf of a latch circuit 96. It adds. Moreover, the output of a latch circuit 96 is added in phase data ktheta and an adder circuit 98, and in a phase-shifting circuit 99, the phase of 0 times or the phase shift of 90 degrees is given, and the output is read to the sinusoidal memory 101, and is supplied as the address. It is latched to a latch circuit 103 by the signal with which the level of each sample point of a sinusoidal form is memorized by the sinusoidal memory 101, and that digital sinusoidal signal by which reading appearance was carried out was latched to the latch circuit 102 by the latch command to a latch circuit 26, and the phase shifted about 180 degrees to this latch command. The output of a latch circuit 102 turns into a digital sine wave output, the output of a latch circuit 103 is latched to the latch and

coincidence to a latch circuit 26 by the latch circuit 104, and a digital cosine wave output is obtained from a latch circuit 104. Frequency data kf Since accumulation is carried out every clock of frequency fR / 2, it is the frequency data kf. A frequency becomes high, so that it is large, and it is the frequency data kf. A frequency becomes low, so that it is small. What is necessary is just to change whether the most significant bit of the input data and the following bit are passed as it is, or what made what took the exclusive OR for them the most significant bit, and reversed the 2nd bit from the most significant is outputted as 2nd bit from the most significant, as shown in drawing 2 B since a phase-shifting circuit 99 is outputted as it is or a phase is shifted and outputted about 90 degrees. Thus, for a frequency, fR xkf/2L+1 and a phase theta are 2pixktheta/2L. A sinusoidal output and a cosine wave output are obtained. fR It is the frequency of the clock which drives a flip-flop 95.

[0015] It returns to explanation of drawing 1 , frequency f1+fa is set up to a synthesizer 93, phase thetaa is set up, the cosine wave output cos {2pi(f1+fa) t+thetaa} is outputted by this, a multiplier 86 is supplied, and the sinusoidal output sin {2pi(f1+fa) andt+thetaa} is outputted, and a multiplier 87 is supplied. On the other hand to a synthesizer 94, frequency f1+fb is set up, phase thetab is outputted, the cosine wave output cos {2pi(f1+fb) andt+thetab} is supplied to a multiplier 91, and the sinusoidal output sin {2pi(f1+fb) andt+thetab} is supplied to a multiplier 92. Each output of multipliers 86 and 87 is supplied to multiplication mold DA converter 105,106, respectively, and each output of multipliers 91 and 92 is supplied to multiplication mold DA converter 107,108, respectively. On the other hand, random noise is generated from the random noise generator 109, and after decreasing the noise with an attenuator 111 if needed, while being added in the direct current voltage and the adder circuit 113 from adjustable DC power supply 112, supplying the output of the adder circuit 113 to each criteria power supply terminal of multiplication mold DA converter 105,106 as Rayleigh noise A(t) and multiplying by it with the input digital signal, the digital signal is changed into an analog signal. The noise from a noise generator 109 is similarly supplied to an adder 115 through an attenuator 114, the output direct current voltage of adjustable DC power supply 116 is added, the output from an adder 115 is supplied to the criteria power supply terminal of multiplier DA converter 107,108 as Rayleigh noise B(t), and while multiplying to the input digital signal, the digital signal is changed by the analog signal.

[0016] each output of DA converter 105,106 -- respectively -- an attenuator 117,118 -- setting -- respectively -- every [Ga] -- it decreases -- having -- moreover, each output from DA converter 107,108 -- an attenuator 119,121 -- setting -- respectively -- GB only -- it decreases. The output of an attenuator 117,119 is added in an adder 122, and is supplied to a multiplier 123, and each output of an attenuator 118,121 is added with an adder 124, and is supplied to a multiplier 125.

[0017] the signal from the reference signal generator 126 -- frequency fR it is -- while synthesizers 93 and 94 are supplied as a clock, respectively, dividing of the output is carried out to 1 for an integer by the counting-down circuit 127, while the clock generation machine 27 for data generating is supplied, it is supplied as a shift clock to the sign delay means 72, and each part is supplied as a clock for other digital processings. Furthermore, the output of the reference signal generator 126 is supplied to a phase locked loop (PLL) 128 as a reference signal. In the PLL128, it is carrier frequency f0-f1. A setting-out input is carried out. Frequency f0-f1 which synchronized with the reference signal Signal cos {2pi(f0-f1) -t} is outputted, and while this is supplied to a multiplier 123 as a carrier signal, a multiplier 125 is supplied through a phase shifter 129 90 degrees. The output of a multiplier 123,125 is added with an adder 131, and the addition output is decreased with an attenuator 132, and is outputted to an output terminal 133. The multiplier 123,125, the phase shifter 129, and the adder 131 constitute the quadrature modulation circuit 134. Moreover, it is the output carrier frequency of PLL128 f0-f1 What is carried out is the carrier frequency f0 of the output signal of an output terminal 133. It is necessary to increase or to decrease. that is, -- since a negative frequency cannot be generated in synthesizers 93 and 94 -- f1 only -- as a high frequency It is a core f0 about the frequency of an output subcarrier [in / by this / forward and the negative frequencies fa and fb can be freely chosen to it, and / the quadrature modulation circuit 13]. It can receive and only fa and fb can

change to forward and negative.
[0018] In this configuration, a shift register is used for the sign delay means 72, and it is fd about that shift frequency. If it carries out and the shift stage where an output is taken out is set to na and nb, the sign information supplied to the coordinate transformation means 82 and 83 is thetaA, respectively. (t) =theta (t−na/fd) and thetaB It is set to (t) =theta (t−nb/fd). Therefore, the signal outputted with a terminal 133 is as follows.
[0019] Gc− [2pi (f0+fa) and Ga−A(t) and cos {t+theta a+theta (t−na/fd)} +Gb−B (t), and cos {2pi (f0+fb) and t+theta b+theta (t−nb/fd)}]
In the case of a phasing simulation, it is two modulation−codes [the same shift stage in the sign election means 72 to] thetaA. (t) and thetaB (t) is obtained or it is modulation−code thetaA. (t) and thetaB (t) shifts the amount of delay only in the condition of maintaining correlation. Rayleigh scattering over the path of two electric waves is given as A (t) and B (t), and a value with each Doppler shift respectively small as fa and fb in the first electric−wave path and second electric−wave path is given. The phase contrast of the two electric−wave paths is determined by setting−out phase thetaa in the digital synthesizers 93 and 94, and thetab, the Rayleigh noise is given by A (t) and B (t), and the magnitude of attenuation is changed by the attenuator 117,119. The time delay of the first electric−wave path is given by {(na/fd) −thetaa / 2pi (f0+fa)}, and the time lag of the second electric−wave path is given by {(nb/fd) −thetab / 2pi (f0+fb)}. The signal with which each part was controlled and the phasing effectiveness was given like the conventional technique can be acquired by doing in this way.
[0020] Moreover, two signals thetaA which sets for the sign delay means 27 and is outputted more when acquiring the interference signal between adjacent channels (t) and thetaB In order that (t) may make the difference of the amount of delay size mutually at extent without correlation and may obtain the delta frequency between channels in the condition, a part of setting−out frequency fa and fb of synthesizers 93 and 94 is detached enough mutually. Also in this case, the simulation of the interference signal between adjacent channels can be carried out as usual.
[0021] In ****, the simulation of multi−pass phasing and the interference simulation between other a large number channels can be performed by preparing two or more groups of the coordinate transformation means 82, filters 84 and 85, multipliers 86 and 87, DA converter 105,106, an attenuator 111, an adder 113, an attenuator 117,118, and a power source 112. Moreover, in ****, although the phasing simulation about a pai−fourth−Differential−QPSK modulating signal was performed, the simulation of phasing to other communication modes or interference between adjacent channels can also be performed by changing a modulator 71.
[0022]
[Effect of the Invention] In order to make in digital one using the difference of the delay [according to / like / this invention / in / for the difference of two paths, or the difference of the signal path of adjacent channel interference / the sign delay means 72] which stated above, the difference of the setting−out phase in frequency synthesizers 93 and 94, etc., Since the delay line is not used like before, it is not influenced by fluctuation of ambient temperature, and it reaches far and wide and it is [it is stable to temperature or frequency change and] possible continuous and to perform a transit delay simulation without distortion. Moreover, since processing of Rayleigh scattering or a Doppler shift is realized in digital one on the comparatively low frequency, the balanced modulator and phase shifter in a high frequency are good only only in the quadrature modulation circuit 134 in a tail end, and, therefore, the adjustment to a frequency is easy for them.

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TECHNICAL FIELD

[Industrial Application] This invention is used in order to evaluate receiving engine performance, such as digital migration communication system, and receive Rayleigh scattering, a Doppler shift is received, or it relates phasing to the phasing simulator generated on real time in the signal of a carrier beam condition, and the same signal.

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PRIOR ART

[Description of the Prior Art] The conventional phasing simulator is shown in drawing 3 . In-phase signal I (t) and rectangular signal Q (t) is added to the quadrature modulation machine 11, and the modulation output is changed into the real part and imaginary part in the coordinate transformation machine 12 changed into rectangular coordinates from a polar coordinate (division). The real part and imaginary part which were these-changed are supplied to DA converters 15 and 16 of a multiplication mold respectively through the digital low pass filters 13 and 14, respectively. The output voltage of adjustable DC power supply 17 is impressed to the source of reference voltage of DA converters 15 and 16, and it is direct current voltage VA. It multiplies.
[0003] The output of these DA converters 15 and 16 is supplied to multipliers 18 and 19, respectively. Frequency fA from a sine wave oscillator 21 While a subcarrier output is supplied to a multiplier 18 as it is, a multiplier 19 is supplied through a phase-shifting circuit 22 90 degrees. The output of these multipliers 18 and 19 is added with an adder 23, and it multiplies by the addition output, i.e., a quadrature modulation output, in a multiplier 24 with noise A (t) by which the noise from the random noise generator 25 was made suitable level with the attenuator 26. the signal with which this noise was imposed -- an attenuator 27 -- GA only -- it decreases -- having -- that decreased output -- the adjustable delay means 28 -- tA only -- while being delayed and supplying a multiplier 29, a multiplier 32 is supplied through a phase shifter 31. It is a frequency f1 from the sine oscillator 33. While a signal is supplied to a multiplier 29, a multiplier 32 is supplied through a phase shifter 34 90 degrees. The output of multipliers 29 and 32 is added with an adder 35.
[0004] On the other hand, the output of an adder 23 branches and is supplied also to a multiplier 37 through the stationary-contact F side of a changeover switch 36. The noise from a noise generator 25 is given to the multiplier 37 as noise B (t) through the attenuator 38. the output of this multiplier 37 -- an attenuator 39 -- GB only -- it decreases -- having -- further -- that attenuation output -- the adjustable delay means 41 -- tB only -- it is delayed and a multiplier 42 is supplied. Frequency f2 While the output of the oscillator 43 which generates a sine wave is supplied to a multiplier 42, a multiplier 45 is supplied through a phase shifter 44 90 degrees, and as for the output of the delay means 41, a multiplier 45 is also supplied through the phase shifter 46. Each output of multipliers 42 and 45 is added with an adder 47. each output of adders 35 and 47 adds with an adder 48 -- having -- the addition output -- an attenuator 49 -- GC only -- in response to attenuation, it is outputted to an output terminal 51.
[0005] Moreover, in-phase signal I' (t) and rectangular signal Q' (t) carry out quadrature modulation of the subcarrier in the quadrature modulation machine 52, in the coordinate transformation machine 53, the modulation output is changed into real part and imaginary part, and is taken out, and these real part and imaginary part are supplied to DA converters 56 and 57 of a multiplication mold respectively through the digital low pass filters 54 and 55. In DA converters 56 and 57, it is an electrical potential difference VB from the adjustable power source 58. It is impressed by the criteria power supply terminal, and is VB. It multiplies. Multipliers 59 and 61 are supplied and each output of DA converters 56 and 57 is the frequency fB from an oscillator 62, respectively. While a subcarrier is supplied to a multiplier 59, a multiplier 61 is

supplied through a phase shifter 63 90 degrees. The output of multipliers 59 and 61 is added with an adder 64, and the addition output is supplied to a multiplier 37 through the stationary-contact I side of a changeover switch 36.

[0006] In the communication link between a mobile station, a fixed station, or a mobile station, a direct wave and a reflected wave are received simultaneously, and moreover, as for the reflected wave, level and a phase are changed, or two or more reflected waves are mainly received. For this reason, an input signal becomes that to which level and a phase were changed. Moreover, received frequency is changed by the so-called Doppler shift by the relative movement between a mobile station and a fixed station. For carrying out the simulation (phasing simulation) of these fluctuation condition, the changeover switch 36 is connected to the stationary-contact F side. The output signal acquired by the output terminal 51 at this time is expressed with a degree type.

[0007] GC - [-- GA - A -- (-- t --) - cos -- {-- two -- pi (fA+f1) - (t-tA) -- + -- theta -- A -- (-- t --) --} - VA -- + -- GB - B -- (-- t --) - cos -- {-- two -- pi (fA+f2) - (t-tB) -- + -- theta -- A -- (-- t --) --} - VA --]

A (t) is Rayleigh scattering of the first path of an electric wave, and its B (t) is equivalent to Rayleigh scattering of the second path of an electric wave here. Moreover, the magnitude of attenuation GA and GB It is the magnitude of attenuation of the second path for a start, respectively. fA It is carrier frequency and is f1 and f2. It is a Doppler shift frequency in the second path for a start, respectively. Moreover, thetaA (t) is transmit information. Furthermore, they are tA and tB. It is the time lag of the second path for a start, respectively. therefore, the magnitude of attenuation of these each part or the amount tA of delay of the delay means 28 and 41, and tB again -- a frequency f1 and f2 etc. -- making it change -- various conditions -- that is, a carrier beam condition can be actually simulated for phasing.

[0008] For, simulating interference between adjacent channels on the other hand, a changeover switch 36 is connected to a stationary-contact I side. The output of the output terminal 51 in this condition is expressed with a degree type.

GC - [-- GA - A -- (-- t --) - cos -- {-- two -- pi (fA+f1) - (t-tA) -- + -- theta -- A -- (-- t --) --} - VA -- + -- GB - B -- (-- t --) - cos -- {-- two -- pi (fB+f2) - (t-tB) -- + -- theta -- B -- (-- t --) --} - VB --]

It is thetaB here. (t) is the transmit information by the side of Channel B. fB It is the carrier frequency by the side of Channel B. In this case, it sets between adjacent channels and carrier frequency is fA+f1. fB+f2 It becomes interference of a between, and these time amount thru/or phases is adjusted by the delay means 28 and 41, and that frequency difference is f1, f2, fA, and fB. It is changed and level is GA and GB. It is changed.

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EFFECT OF THE INVENTION

[Effect of the Invention] In order to make in digital one using the difference of the delay [according to / like / this invention / in / for the difference of two paths, or the difference of the signal path of adjacent channel interference / the sign delay means 72] which stated above, the difference of the setting-out phase in frequency synthesizers 93 and 94, etc., Since the delay line is not used like before, it is not influenced by fluctuation of ambient temperature, and it reaches far and wide and it is [it is stable to temperature or frequency change and] possible continuous and to perform a transit delay simulation without distortion. Moreover, since processing of Rayleigh scattering or a Doppler shift is realized in digital one on the comparatively low frequency, the balanced modulator and phase shifter in a high frequency are good only only in the quadrature modulation circuit 134 in a tail end, and, therefore, the adjustment to a frequency is easy for them.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] Although the adjustable delay means 28 and 41 are used in the former in order to change two path differences, they are this time delay tA and tB. It is difficult for a time delay to change according to temperature fluctuation, since the time delay of a line ******** cable is usually used for obtaining, and for delay distortion to arise with a frequency and to change a time delay with large range with still higher resolution.
[0010] Moreover, since it is used, many the balanced modulators 18, 19, 24, 29, 32, 37, 42, 45, 59, and 61, i.e., the multipliers, of high frequency, and the phase shifter of much more RFs is used, the adjustment to a frequency is difficult. And two systems were used and the configuration was complicated.

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MEANS

[Means for Solving the Problem] According to this invention, a transmitting sign is delayed from a sign delay means in step. The first real part, the first imaginary part and the second real part, and the second imaginary part about each sign of the two delay outputs The first, It is changed by the second coordinate operator stage. These first real part and the first imaginary part, respectively with the cosine wave output from the first digital synthesizer, and a sinusoidal output The first, It multiplies with the second multiplication means, and for a start [these], the output of the second multiplication means is changed into an analog signal, respectively while a noise is imposed by the second multiplication mold DA translation means for a start. on the other hand, the cosine wave output and the sinusoidal output from the second digital synthesizer multiply by the second real part and the second imaginary part with the third and fourth multiplication means, respectively -- having -- these third and fourth multiplication output -- the third and fourth multiplication mold DA translation means -- the above -- things -- it is changed into an analog signal while a noise multiplies. For a start, the output of the third DA translation means is added with the first addition means, the output of the second, third, and fourth DA translation means is added with the second addition means, and quadrature modulation of the output of the second addition means is carried out with a quadrature modulation means for a start [these].

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EXAMPLE

[Example] The example of this invention is shown in drawing 1 . Transmit information [from the quadrature modulation machine 71] theta (t) is supplied to the sign delay means 72, and the sign unit, i.e., step-delay, is performed. As for the sign delay means 72, a shift register, a FIFO memory, etc. are used. Moreover, as a quadrature modulation machine 71, dividing of the clock for data generating from the clock generation machine 73 for data generating is carried out to one half with a counting-down circuit 74, counting of the dividing output is carried out with an address counter 75, the memory 76 for inphases and the memory 77 for a rectangular cross are read considering the enumerated data of the address counter 75 as the address, respectively, and in-phase signal I (t) and rectangular signal Q (t) is outputted. both [these] outputs supply a modulator 81 through changeover switches 78 and 79, respectively -- having -- subcarrier length -- for example, a pai-fourth-Differential-QPSK modulation is carried out. Switches 78 and 79 are changed when inputting the in-phase signal and the rectangular signal from the outside.
[0013] the sign delay means 72 -- respectively -- a sign unit -- things -- delay was given or the signal with which the same delay was given is outputted. The output from a tap (shift stage) which is different when the sign delay means 72 is a shift register, or the output from the same tap (shift stage) is sign transmit information thetaA, respectively. (t) and thetaB It is taken out as (t) and the coordinate transformation means 82 and 83 are supplied. In the coordinate transformation means 82 and 83, conversion of a polar coordinate and rectangular coordinates is performed and, as for each input sign, real part and imaginary part are outputted, respectively. The real part and imaginary part from the coordinate transformation means 82 are supplied to multipliers 86 and 87 through the FIR form digital low pass filters 84 and 85 if needed, respectively. Moreover, the real part and imaginary part from the coordinate transformation means 83 are supplied to multipliers 91 and 92 through the FIR form digital low pass filters 88 and 89 if needed, respectively.
[0014] On the other hand, the digital synthesizers 93 and 94 are formed. The digital synthesizers 93 and 94 are constituted, as it can change and a phase and a frequency are shown in drawing 2 A, respectively. Namely, frequency fR from the flip-flop 95 of a toggle mold While was set to one half and the output of an adder 97 is latched to a latch circuit 96 with an output. An adder 97 is the output and the frequency data kf of a latch circuit 96. It adds. Moreover, the output of a latch circuit 96 is added in phase data ktheta and an adder circuit 98, and in a phase-shifting circuit 99, the phase of 0 times or the phase shift of 90 degrees is given, and the output is read to the sinusoidal memory 101, and is supplied as the address. It is latched to a latch circuit 103 by the signal with which the level of each sample point of a sinusoidal form is memorized by the sinusoidal memory 101, and that digital sinusoidal signal by which reading appearance was carried out was latched to the latch circuit 102 by the latch command to a latch circuit 26, and the phase shifted about 180 degrees to this latch command. The output of a latch circuit 102 turns into a digital sine wave output, the output of a latch circuit 103 is latched to the latch and coincidence to a latch circuit 26 by the latch circuit 104, and a digital cosine wave output is obtained from a latch circuit 104. Frequency data kf Since accumulation is carried out every clock of frequency fR / 2, it is the frequency data kf. A frequency becomes high, so that it is large, and it is the frequency data kf. A frequency becomes low, so that it is small. What is

necessary is just to change whether the most significant bit of the input data and the following bit are passed as it is, or what made what took the exclusive OR for them the most significant bit, and reversed the 2nd bit from the most significant is outputted as 2nd bit from the most significant, as shown in drawing 2 B since a phase-shifting circuit 99 is outputted as it is or a phase is shifted and outputted about 90 degrees. Thus, for a frequency, fR xkf/2L+1 and a phase theta are 2pixktheta/2L. A sinusoidal output and a cosine wave output are obtained. fR It is the frequency of the clock which drives a flip-flop 95.

[0015] It returns to explanation of drawing 1 , frequency f1+fa is set up to a synthesizer 93, phase thetaa is set up, the cosine wave output cos {2pi(f1+fa) t+thetaa} is outputted by this, a multiplier 86 is supplied, and the sinusoidal output sin {2pi(f1+fa) andt+thetaa} is outputted, and a multiplier 87 is supplied. On the other hand to a synthesizer 94, frequency f1+fb is set up, phase thetab is outputted, the cosine wave output cos {2pi(f1+fb) andt+thetab} is supplied to a multiplier 91, and the sinusoidal output sin {2pi(f1+fb) andt+thetab} is supplied to a multiplier 92. Each output of multipliers 86 and 87 is supplied to multiplication mold DA converter 105,106, respectively, and each output of multipliers 91 and 92 is supplied to multiplication mold DA converter 107,108, respectively. On the other hand, random noise is generated from the random noise generator 109, and after decreasing the noise with an attenuator 111 if needed, while being added in the direct current voltage and the adder circuit 113 from adjustable DC power supply 112, supplying the output of the adder circuit 113 to each criteria power supply terminal of multiplication mold DA converter 105,106 as Rayleigh noise A(t) and multiplying by it with the input digital signal, the digital signal is changed into an analog signal. The noise from a noise generator 109 is similarly supplied to an adder 115 through an attenuator 114, the output direct current voltage of adjustable DC power supply 116 is added, the output from an adder 115 is supplied to the criteria power supply terminal of multiplier DA converter 107,108 as Rayleigh noise B(t), and while multiplying to the input digital signal, the digital signal is changed by the analog signal.

[0016] each output of DA converter 105,106 -- respectively -- an attenuator 117,118 -- setting -- respectively -- every [Ga] -- it decreases -- having -- moreover, each output from DA converter 107,108 -- an attenuator 119,121 -- setting -- respectively -- GB only -- it decreases. The output of an attenuator 117,119 is added in an adder 122, and is supplied to a multiplier 123, and each output of an attenuator 118,121 is added with an adder 124, and is supplied to a multiplier 125.

[0017] the signal from the reference signal generator 126 -- frequency fR it is -- while synthesizers 93 and 94 are supplied as a clock, respectively, dividing of the output is carried out to 1 for an integer by the counting-down circuit 127, while the clock generation machine 27 for data generating is supplied, it is supplied as a shift clock to the sign delay means 72, and each part is supplied as a clock for other digital processings. Furthermore, the output of the reference signal generator 126 is supplied to a phase locked loop (PLL) 128 as a reference signal. In the PLL128, it is carrier frequency f0-f1. A setting-out input is carried out. Frequency f0-f1 which synchronized with the reference signal Signal cos {2pi(f0-f1) -t} is outputted, and while this is supplied to a multiplier 123 as a carrier signal, a multiplier 125 is supplied through a phase shifter 129 90 degrees. The output of a multiplier 123,125 is added with an adder 131, and the addition output is decreased with an attenuator 132, and is outputted to an output terminal 133. The multiplier 123,125, the phase shifter 129, and the adder 131 constitute the quadrature modulation circuit 134. Moreover, it is the output carrier frequency of PLL128 f0-f1 What is carried out is the carrier frequency f0 of the output signal of an output terminal 133. It is necessary to increase or to decrease. that is, -- since a negative frequency cannot be generated in synthesizers 93 and 94 -- f1 only -- as a high frequency It is a core f0 about the frequency of an output subcarrier [in / by this / forward and the negative frequencies fa and fb can be freely chosen to it, and / the quadrature modulation circuit 13]. It can receive and only fa and fb can change to forward and negative.

[0018] In this configuration, a shift register is used for the sign delay means 72, and it is fd about that shift frequency. If it carries out and the shift stage where an output is taken out is set to na and nb, the sign information supplied to the coordinate transformation means 82 and 83 is

thetaA, respectively. (t) =theta (t−na/fd) and thetaB It is set to (t) =theta (t−nb/fd). Therefore, the signal outputted with a terminal 133 is as follows.

[0019] Gc− [2pi (f0+fa) and Ga−A(t) and cos {t+theta a+theta (t−na/fd)} +Gb−B (t), and cos {2pi (f0+fb) and t+theta b+theta (t−nb/fd)}]

In the case of a phasing simulation, it is two modulation−codes [the same shift stage in the sign election means 72 to] thetaA. (t) and thetaB (t) is obtained or it is modulation−code thetaA. (t) and thetaB (t) shifts the amount of delay only in the condition of maintaining correlation. Rayleigh scattering over the path of two electric waves is given as A (t) and B (t), and a value with each Doppler shift respectively small as fa and fb in the first electric−wave path and second electric−wave path is given. The phase contrast of the two electric−wave paths is determined by setting−out phase thetaa in the digital synthesizers 93 and 94, and thetab, the Rayleigh noise is given by A (t) and B (t), and the magnitude of attenuation is changed by the attenuator 117,119. The time delay of the first electric−wave path is given by {(na/fd) −thetaa / 2pi (f0+fa)}, and the time lag of the second electric−wave path is given by {(nb/fd) −thetab / 2pi (f0+fb)}. The signal with which each part was controlled and the phasing effectiveness was given like the conventional technique can be acquired by doing in this way.

[0020] Moreover, two signals thetaA which sets for the sign delay means 27 and is outputted more when acquiring the interference signal between adjacent channels (t) and thetaB In order that (t) may make the difference of the amount of delay size mutually at extent without correlation and may obtain the delta frequency between channels in the condition, a part of setting−out frequency fa and fb of synthesizers 93 and 94 is detached enough mutually. Also in this case, the simulation of the interference signal between adjacent channels can be carried out as usual.

[0021] In ****, the simulation of multi−pass phasing and the interference simulation between other a large number channels can be performed by preparing two or more groups of the coordinate transformation means 82, filters 84 and 85, multipliers 86 and 87, DA converter 105,106, an attenuator 111, an adder 113, an attenuator 117,118, and a power source 112. Moreover, in ****, although the phasing simulation about a pai−fourth−Differential−QPSK modulating signal was performed, the simulation of phasing to other communication modes or interference between adjacent channels can also be performed by changing a modulator 71.

[Translation done.]

* NOTICES *

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1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The block diagram showing the example of this invention.
[Drawing 2] The block diagram in which A shows the example of a digital synthesizer, and B are the block diagrams showing the phase-shifting circuit 99.
[Drawing 3] The block diagram showing the conventional phasing simulator.

[Translation done.]